REMARKS/ARGUMENTS

This Amendment is in response to the non-final Office Action dated August 7, 2008. In this Amendment, claims 1-3 and 5 have been amended, no claims have been canceled, and no new claims are presented.

I. TECHNICAL AMENDMENTS

Amendments have been made to claims 1-3 and 5 in order to ensure proper grammar and antecedent bases. For example, "digital integrated circuit" has been amended to "integrated circuit" in claims 2 and 3, and "the voltage" has been amended to "a voltage" in claim 5. Such amendments, unless otherwise discussed below, are not intended, and should not be interpreted, as limiting amendments but are merely made to ensure compliance with U.S. statutory formalities.

II. CLAIM REJECTIONS UNDER 35 U.S.C. § 112 ¶ 2

The Office Action rejected claim 1 under 35 U.S.C. § 112 paragraph 2 because the claim recited "if the external test circuitry is free from maintaining the integrated circuit in a test mode" but did not explicitly recite the other condition, *i.e.,* if the external test circuitry is not free from maintaining the integrated circuit in a test mode. While Applicant believes that there is no requirement under 35 U.S.C. § 112 ¶ 2, related case law, 37 C.F.R., the MPEP, or USPTO guidelines which necessitates the recitation of each alternate condition in a claim, claim 1 has been amended to recite "otherwise, when the integrated circuit is in the test mode and the input signal on the input/output pin is not in the second range for the second predetermined finite period of time, the integrated circuit continues to operate in the test mode" (emphasis added). Support for this can be found in the application, for example in paragraphs [0028] and [0029] of the specification. Accordingly, Applicant respectfully requests withdrawal of the § 112 ¶ 2 rejection.

III. CLAIM REJECTIONS UNDER 35 U.S.C. § 103

The Office Action rejected claims 1, 2, and 5 under 35 U.S.C. § 103(a) as being unpatentable (obvious) over Toyofuku et al. (JP 57-133656) (hereinafter "Toyofuku") in view of Ishikawa (US 4,638,247) (hereinafter "Ishikawa"). Claim 3 was rejected under § 103(a) as being unpatentable over Toyofuku and Ishikawa, and further in view of Stewart et al. (US 4,947,357) (hereinafter "Stewart"). Claim 4 was rejected under § 103(a) as being unpatentable over Toyofuku and Ishikawa, and further in view of Davies, Jr. (US 4,449,065) (hereinafter "Davies, Jr."). Claim 6 was rejected under § 103(a) as being unpatentable over Toyofuku and Ishikawa, and further in view of Wise et al. (US 5,404,304) (hereinafter "Wise"). Applicant respectfully traverses the § 103 rejections.

Claim 1 is patentably distinguished over the combination of Toyofuku and Ishikawa in at least that the interface element can communicate with external test circuitry via a single input/output pin. Toyofuku describes an interface element for an integrated circuit for interfacing the external test circuitry; however, Toyofuku requires two input signals – one from the multifunction input terminal (IN2, Toyofuku, Figs. 2 and 5) and another reset signal (R, Toyofuku, Figs. 2, 4 and 5). Presumably, the motivation for the invention disclosed in Toyofuku was that by using two input sources, IN2 and R, the test mode could be initiated by a pulse provided by input IN2 and it could be aborted by a pulse provided by input R (*see, e.g.,* Toyofuku, Abstract and Fig. 4), rather than requiring a fixed level to be inputted to the input terminal at all times when in the test mode (*see* Toyofuku, Abstract and Fig. 3). Therefore, the use of two input signals was apparently central to the invention disclosed by Toyofuku. Accordingly, Toyofuku does not disclose or suggest how such an interface element for an integrated circuit for interfacing with external test circuitry which communicates with external test circuitry via a "single input/output pin" (claim 1) could be achieved. Likewise, Ishikawa does not disclose, teach, or suggest a "single pin . . . operat[ing] with several logic thresholds and wherein if an input signal on the input/output pin is in a first range defined by the logic thresholds for a first predetermined finite period of time after a power on reset, the integrated circuit is placed in a test mode" (claim 1). As such, amended claim 1 and dependent claims 2-6 are patentably distinguished with respect to Toyofuku in view of Ishikawa.

Notwithstanding the above, claim 1 is further distinguished over the combined teachings of Toyofuku and Ishikawa by at least the following limitation: when the integrated circuit is in test mode, "if the input signal . . . is in a second range defined by the logic thresholds for a second predetermined finite period of time, the integrated circuit defaults from the test mode to a normal mode," otherwise the integrated circuit continues to operate in the test mode. While the Office Action concedes that this is not disclosed by Toyofuku, the Office Action claims that it is disclosed by Ishikawa. However, Ishikawa does not disclose or suggest such a limitation. The passage cited in the Office Action (Ishikawa column 4, lines 50-57) merely discloses an integrated circuit which is operative to produce normal drive control signals in the absence of a test signal. Thus, once in test mode, the invention disclosed in Ishikawa requires that all of the test terminals (53, Ishikawa, Fig. 5) are opened. Ishikawa does not disclose or suggest how such an integrated circuit, once in test mode, might automatically revert back or otherwise default to the normal mode of operation "if the input signal on the input/output pin is in a second range . . . for a second predetermined finite period of time" (claim 1). As such, claim 1 and the dependent claims 2-6 of the present invention are patentably distinguished with respect to Toyofuku in view of Ishikawa.

Finally, claim 1 is further distinguished over the combined teachings of Toyofuku and Ishikawa by at least the following limitation: if the "input signal on the input/output pin is in a first range defined by the logic thresholds for a first predetermined finite period of time after a power on reset, the integrated circuit is placed in a the test mode" (claim 1). This is neither disclosed nor suggested by either prior art document. The mechanism for switching to a test mode disclosed in Toyofuku apparently is a flip-flop, such that *as soon as* the voltage applied to the multifunctional input terminal, IN2, exceeds VCC, the integrated circuit switches to test mode. The mechanism for switching to test mode disclosed in Ishikawa is such that *as soon as* at least one of the test terminals (53, Ishikawa, Fig. 5) is closed, the integrated circuit switches to test mode. Therefore, neither prior art document discloses the limitation. Thus, claim 1 and dependent claims 2-6 of the present application are patentably distinguished with respect to the combination of Toyofuku and Ishikawa, as well as further in view of the other relied-upon references.

Each of the claims dependent on claim 1 is patentably distinguished from the combined teachings of Toyofuku and Ishikawa by at least the limitations discussed above. Stewart, Davies Jr., and Wise also do not teach or suggest such limitations. As such, dependent claims 2-6, which were each rejected using a combination of Toyofuku in view of Ishikawa, are novel and nonobvious with respect to Toyofuku in view of Ishikawa as well as Stewart, Davies Jr., and Wise where applied. Accordingly, Applicant respectfully requests withdrawal of the § 103 rejections.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 472-5000.

Respectfully submitted,

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